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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/671,436	09/27/2000	Yoshinari Matsuda	09792909-0425	6069

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EXAMINER

LEVI, DAMEON E

ART UNIT	PAPER NUMBER
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2841

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/671,436

Applicant(s)

MATSUDA ET AL.

Examiner

Dameon E Levi

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11/29/2004 RCE.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Fushie et al US Patent 6339197.

Regarding claim 1, Fushie et al discloses a printed circuit board comprising:

a glass substrate(for example, see element 2, Figs 1-6C, 20, Figs 7A-8B, 32, Figs 9A-12B) provided with through-holes(for example, see elements 3, Figs 1-6C) , conductive patterns(for example, see elements 6, Figs 1-6C) provided on both surfaces of the glass substrate in such a manner as to be made conductive to each other via the through-holes, and a sealing member(for example, see element 8, Figs 1-6C) provided to fill the

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through holes, the sealing member being operable to inhibit moisture permeation through the through holes .

Moreover the limitation,(the sealing member being operable to inhibit moisture permeation through the through holes) is an intended use recitation of the sealing member and has not been accorded patentable weight by the Office.

Regarding claim 2, Fushie et al discloses wherein the glass substrate is a no-alkali glass substrate(for example, see Fig 7A).

Regarding claim 3, Fushie et al discloses wherein the sealing member is a conductive paste containing an epoxy resin as a binder(for example, see element 8, Figs 1-6C)

Regarding claim 4, Fushie et al discloses wherein a conductive film is provided on an inner wall surface of each of the through-holes in such a manner as to connect the conductive patterns provided on both surfaces of the glass substrate to each other, and an inner space, inside the conductive film, of the through-hole is filled with the sealing member (for example, see elements 3,8 Figs 1-6C)

Regarding claim 5, Fushie et al discloses wherein the sealing member is an epoxy resin(for example, see elements 8, Figs 1-6C)

Regarding claim 6, Fushie et al discloses wherein the surface of the sealing member exposed from each of the through-holes is covered with a metal film (for example, see elements 3,8 Figs 1-6C)

Regarding claim 7, Fushie et al discloses a printed wiring board comprising:
a glass substrate(for example, see element 2, Figs 1-6C, 20, Figs 7A-8B, 32, Figs 9A-12B) provided with a plurality of through-holes(for example, see elements 3, Figs 1-6C);

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a plurality of conductive patterns (for example, see elements 6, Figs 1-6C) provided on both surfaces of said glass substrate in such a manner as to be made conductive to each other via said through-holes; and a sealing member (for example, see element 8, Figs 1-6C) provided to fill said through-holes, wherein each of said conductive patterns has a stacked structure of a chromium film and a copper film formed thereon (for example, see elements 5a, 5b, 5c, 35a, 35b, 35c Figs 1-14).

Regarding claim 8, Fushie et al discloses wherein each of said conductive patterns has a stacked structure of an epoxy resin film and a copper film formed thereon (for example, see element 35a, 35b, 35c, Figs 1-14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fushie et al US Patent 6339197 in view of Stevens US Patent 6392356 and further in view of Nakazawa et al US Patent 6411349

Regarding claim 9, Fushie et al discloses a device comprising:

a printed wiring board including a glass substrate (for example, see element 2, Figs 1-6C, 20, Figs 7A-8B, 32, Figs 9A-12B) provided with through-holes (for example, see elements 3, Figs 1-6C),

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conductive patterns(for example, see elements 6, Figs 1-6C) provided on both surfaces of the glass substrate in such a manner as to be made conductive to each other via the through holes, and a first sealing member(for example, see element 8, Figs 1-6C) provided to fill the through-holes;

Stevens et al discloses a display device assembly comprising

- a display device provided on one surface of the printed wiring board in such a manner as to be connected to a conductive pattern provided on a one surface of a printed wiring board(for example, see elements 30, Fig 3)
- a drive component for driving the display device, the drive component being disposed on the other surface of the printed wiring board in such a manner as to be connected to the conductive pattern provided on the other surface of the printed wiring board(for example, see elements 70,72, Figs 1-3, see column 5, lines 5-25)

Nakazawa et al discloses a display device assembly wherein

- a second sealing member provided in such a manner as to surround a display device while being in contact with a printed wiring board and a protective glass board (for example, see element 252, Fig 12)

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the glass circuit board as taught by Fushie et al and to arrange the display device components as taught by Stevens for the purpose of achieving a denser array of driver components in order to increase pixel pitch in the display device and to add the second sealing member as taught by Nakazawa et al for

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the purpose vacuum sealing the assembly as a whole.

Regarding claim 10, Fushie et al disclose the instant wherein the glass substrate is a no-alkali glass substrate(for example, see Fig 7A)

Regarding claim 11, Fushie et al discloses wherein the sealing member is a conductive

paste containing an epoxy resin as a binder (for example, see element 8, Figs 1-6C)

Regarding claim 12, Fushie et al discloses wherein a conductive film is provided on an inner wall surface of each of the through-holes in such a manner as to connect the conductive patterns provided on both surfaces of the glass substrate to each other, and an inner space, inside the conductive film, of the through-hole is filled with the sealing member (for example, see elements 3,8 Figs 1-6C)

Regarding claim 13, Fushie et al discloses wherein the sealing member is an epoxy resin(for example, see elements 8, Figs 1-6C)

Regarding claim 14, Fushie et al discloses wherein the surface of the sealing member exposed from each of the through-holes is covered with a metal film (for example, see elements 3,8 Figs 1-6C)

Regarding claim 15, Fushie et al discloses a device comprising:

- a printed wiring board including a glass substrate(for example, see element 2, Figs 1-6C, 20, Figs 7A-8B, 32, Figs 9A-12B) provided with through-holes(for example, see elements 3, Figs 1-6C), conductive patterns (for example, see elements 6, Figs 1-6C) provided on both surfaces of the glass substrate in such a manner as to be made conductive to each other via the through holes, and a first

sealing member(for example, see element 8, Figs 1-6C) provided to fill the through-holes;

Stevens et al discloses a display device assembly comprising

- bumps provided on a conductive pattern provided on one surface of a printed wiring board; a protective glass board disposed in such a manner as to face to the one surface of the printed wiring board; a display device provided on the surface, facing to the printed wiring board, of the protective glass board in such a manner as to be connected to the bumps(for example, see elements 60,12,30 Fig 3)
- a drive component for driving the display device, the drive component being disposed on the other surface of the printed wiring board in such a manner as to be connected to the conductive pattern provided on the other surface of the printed wiring board(for example, see elements 70,72, Figs 1-3, see column 5, lines 5-25)

Nakazawa et al discloses a display device assembly wherein

a second sealing member is provided in such a manner as to surround a display device while being in contact with a printed wiring board and a protective glass board (for example, see element 252, fig 12)

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have include the glass circuit board as taught by Fushie et al and to arrange the display device components as taught by Stevens for the purpose of achieving a denser array of driver components in order to increase pixel pitch in the

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display device and to add the second sealing member as taught by Nakazawa et al for the purpose vacuum sealing the assembly as a whole.

Regarding claim 16, Fushie et al disclose the instant wherein the glass substrate is a no-alkali glass substrate (for example, see Fig 7A)

Regarding claim 17, Fushie et al discloses wherein a conductive film is provided on an inner wall surface of each of the through-holes in such a manner as to connect the conductive patterns provided on both surfaces of the glass substrate to each other, and an inner space, inside the conductive film, of the through-hole is filled with the sealing member (for example, see elements 3,8 Figs 1-6C)

Regarding claim 18, Fushie et al discloses wherein the sealing member is an epoxy resin (for example, see elements 8, Figs 1-6C)

Regarding claim 19, Fushie et al discloses wherein the surface of the sealing member exposed from each of the through-holes is covered with a metal film (for example, see elements 3,8 Figs 1-6C)

Regarding claim 20, Fushie et al discloses a printed wiring board comprising:
a glass substrate (for example, see element 2, Figs 1-6C, 20, Figs 7A-8B, 32, Figs 9A-12B) provided with a plurality of through-holes (for example, see elements 3, Figs 1-6C);
a plurality of conductive patterns (for example, see elements 6, Figs 1-6C) provided on both surfaces of said glass substrate in such a manner as to be made conductive to each other via said through-holes; and a sealing member (for example, see element 8, Figs 1-6C) provided to fill said through-holes, wherein each of said conductive patterns

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has a stacked structure of a chromium film and a copper film formed thereon(for example, see elements 5a,5b,5c, 35a,35b,35c Figs 1-14).

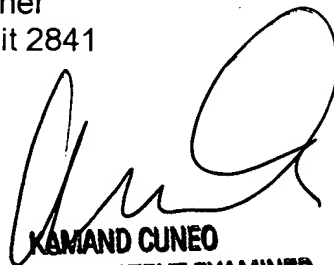
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dameon E Levi whose telephone number is (571) 272-2105. The examiner can normally be reached on Mon.-Fri. (9:00 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DEL

Dameon E Levi
Examiner
Art Unit 2841



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